REMARKS

Reconsideration of the subject application is respectfully requested. This amendment is being filed concurrently with an RCE.

Claims 1-20 were rejected under 35 USC 102 as being anticipated by Goodwin et al. ((U.S. 5,371,870), hereinafter "Goodwin." This rejection is respectfully traversed, especially in view of the forgoing amendments to independent Claims 1, 5, 9, and 13. Dependent Claims 2-4, 6-8, 10-12, and 14-20 have been cancelled in order to expedite prosecution of the subject application.

Each of the independent claims has been amended to recite, in part, that the FIFO memory is read from or written to a plurality of times through the single address in response to the one read or write request from the CPU. This feature is discussed with reference to Fig. 7b of the subject application. See for example, page 8, line 17 continuing to page 9, line 3:

"The 68 clock cycles required for transferring 32 bytes conventionally is reduced as shown in Figure 7B to just 22 clock cycles. Four clock cycles are required initially to establish the source and destination address as before (step 39). However, reading 32 bytes from the memory requires only one instruction fetch for the instruction "Read Multiple" (CM_1) followed by eight read cycles for reading eight blocks (CM_{2-9}), each block having four bytes of data, and one instruction fetch for the instruction "Write Multiple" (CM_{10}) followed by eight write cycles for writing the eight blocks (CM_{11-18}). Accordingly, CPU time is reduced by over two-thirds. As will be readily appreciated, a similar result is obtained for transferring 32 bytes of data from the FIFO."

Only one read or write request, e.g. instruction "Read Multiple" (CM1), from the CPU results in a plurality of read or write accesses, e.g. eight read cycles for reading eight blocks (CM2 - 9) from/to the FIFO memory 22 or 24. This is in distinct contrast to the stream detection logic shown in Fig. 5 of Goodwin. As discussed at column 7, lines 17-27: "This record is kept in a history buffer cache 58, which has eight locations B1-B8; the first location B1 is loaded from the incoming read cache line address through an adder A which adds 1 to the incoming read cache line address (i.e., incrementing) prior to loading into location B1, and when the next read request is received the corresponding cache line address is incremented by adder A before being loaded into location B2, and likewise each subsequent read address received from CPU 10 is incremented and loaded into the next location, proceeding through location B8."

Thus, in Goodwin, the cache memory is accessed only with each next (subsequent) access by the CPU. Goodwin fails to disclose or fairly suggest that the FIFO memory is read from or written to a plurality of times through the single address in response to one read or write request from the CPU, as now specifically recited in each of the independent claims.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration of the present application.

Respectfully submitted,

/Mark P. Watson/
Mark P. Watson
Registration No. 31,448

Please address all correspondence to:

Epson Research and Development, Inc.
Intellectual Property Department
2580 Orchard Parkway, Suite 225
San Jose, CA 95131
Phone: (408) 952-6124
Facsimile: (408) 954-9058
Customer No. 20178

Date: January 9, 2008